What is claimed is:

1. A semiconductor memory device comprising:

first and second bit lines for inputting/outputting complementary data;

a first transistor for controlling connection between a first storage node and the first bit line on the basis of a selection signal;

a second transistor for controlling connection between a second storage node and the second bit line on the basis of the selection signal;

a flip-flop for holding potentials of the first and second storage nodes to output the potentials;

a third transistor, having a channel region given the same potential of the second storage node, to control connection between a first internal node and the first bit line on the basis of the selection signal;

a fourth transistor, having a channel region given the same potential of the second storage node, to control connection between a common potential and the first internal node on the basis of the potential of the second storage node;

a fifth transistor, having a channel region given the same potential of the first storage node, to control connection between a second internal node and the second bit line on the basis of the selection signal; and

a sixth transistor, having a channel region given the same potential of the first storage node, to control connection between the common potential and the second internal node on the basis of the potential of the first storage node.

2. A semiconductor memory device according to claim 1, wherein

the first to sixth transistors are formed on a surface of a semiconductor substrate,

the third and fourth transistors are formed in a first conductivity type well formed in the surface of the semiconductor substrate, and the fifth and sixth transistors are formed in a second conductivity type well formed in the surface of the semiconductor substrate.

3. A semiconductor memory device according to claim 1, wherein

threshold voltages of the first to sixth transistors are almost equal to each other.

4. A semiconductor memory device according to claim 1, wherein

threshold voltages of the first to sixth transistors are lower than a power supply voltage.

5. A semiconductor memory device comprising:

first and second bit lines for inputting/outputting complementary data;

a first transistor to control connection between a first storage node and the first bit line on the basis of a selection signal;

a second transistor to control connection between a second storage node and the second bit line on the basis of the selection signal;

a flip-flop for holding potentials of the first and second storage nodes to output the potentials;

a third transistor, having a channel region given the same potential of the second storage node, to connect a first internal node to the first bit line in a data read state;

a fourth transistor, having a channel region given the same potential of the second storage node, to control connection between a common potential and the first internal node on the basis of the potential of the second storage node;

a fifth transistor, having a channel region given the same potential of the first storage node, to connect a second internal node to the second bit line in a data read state; and

a sixth transistor, having a channel region given the same potential of the first storage node, to control connection between the common potential and the second internal node on the basis of the potential of the first storage node.

6. A semiconductor memory device according to claim 5, wherein

the first to sixth transistors are formed on a surface of a semiconductor substrate,

the third and fourth transistors are formed in a first conductivity type well formed in the surface of the semiconductor substrate, and the fifth and sixth transistors are formed in a second conductivity type well formed in the surface of the semiconductor substrate.

7. A semiconductor memory device according to claim 5, wherein

threshold voltages of the first to sixth transistors are almost equal to each other.

8. A semiconductor memory device according to claim 5, wherein

threshold voltages of the first to sixth transistors are lower than a power supply voltage.

9. A semiconductor memory device comprising:

first and second bit lines for inputting/outputting complementary data;

a first transistor to control connection between a first storage node and the first bit line on the basis of a selection signal;

a second transistor to control connection between a second storage node and the second bit line on the basis of the selection signal;

a flip-flop for holding potentials of the first and second storage nodes to output the potentials;

a third transistor, having a channel region given the same potential of the second storage node, to connect a first internal node to the first bit line in a data read state;

a fourth transistor, having a channel region given the same potential of the second storage node, to control connection between a common potential and the first internal node on the basis of the potential of the second storage node;

a fifth transistor, having a channel region given the same potential of the first storage node, to connect a second internal node to the second bit line in a data read state;

a sixth transistor, having a channel region given the same potential of the first storage node, to control connection between the common potential and the second internal node on the basis of the potential of the first storage node;

a word line connected to the first and second transistors;

a signal line connected to the third and fifth transistors;

a logical circuit for outputting the selection signal to the word line when data is written in the flip-flop and for outputting a control signal for controlling the third and fifth transistors to the signal line in the data read state.

10. A semiconductor memory device according to claim 9, wherein

the logical circuit includes:

a first inverter having an input side to which the selection signal is given;

a second inverter having an input side to which a write control signal for outputting the control signal is given;

a NOR gate having a first input side to which the selection signal is given through the first inverter, having a second input side to which the write control signal is given through the second inverter, and having an output side which is connected to the word line;

an AND gate having a first input side to which the selection signal is given, having a second input side to which the write control signal is given through the second inverter, and having an output side which is connected to gates of the third and fifth transistors.

11. A semiconductor memory device according to claim 9, wherein

the first to sixth transistors are formed on a surface of a semiconductor substrate,

the third and fourth transistors are formed in a first conductivity type well formed in the surface of the semiconductor substrate, and the fifth and sixth transistors are formed in a second conductivity type well formed in the surface of the semiconductor substrate.

12. A semiconductor memory device according to claim 9,

wherein

threshold voltages of the first to sixth transistors are almost equal to each other.

13. A semiconductor memory device according to claim 9, wherein

threshold voltages of the first to sixth transistors are lower than a power supply voltage.